DECLARATION

I, Young-Woo PARK, Korean Patent Attorney of 5F., Seil Building, 727-13, Yeoksam-dong, Gangnam-gu, Seoul, Korea do hereby solemnly and sincerely declare as follows:

1. That I am well acquainted with the English and Korean languages.

2. That the following is a correct translation into English of the accompanying certified copy of Korean Patent Application No. 2002-64554.

and I make the solemn declaration conscientiously believing the same to be true.

Seoul, May 22, 2006

Young-Woo PARK

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This is to certify that annexed hereto is a true copy from the records of the Korean Industrial Property Office of the following application as filed.

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COMMISSIONER

PATENT APPLICATION

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Title of the Invention : **METHOD FOR CLEANING A PROCESSING CHAMBER AND METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE**

[ABSTRACT]

[ABSTRACT]

Disclosed are a method for cleaning a processing chamber, and a method for manufacturing a semiconductor device. Impurities are removed from a substrate in the processing chamber with the plasma of the first gas including hydrogen gas. After the substrate is removed from the processing chamber, the processing chamber is etched with the plasma of a non-hydrogenous second gas. The hydrogen can differently reacts with the material of substrate and the impurities, respectively. Thus, the etching selectivity can be improved and the particles cannot be generated.

[REPRESENTATIVE FIGURE]

FIG. 7

[SPECIFICATION]

[TITLE OF THE INVENTION]

METHOD FOR CLEANING A PROCESSING CHAMBER AND METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE

[BRIEF EXPLANATION OF THE DRAWINGS]

FIG. 1 is a cross-sectional view illustrating the conventional semiconductor device including contact holes;

FIGS. 2 and 3 are cross-sectional views illustrating the conventional process for forming a tungsten plug;

FIG. 4 is an enlarged cross-sectional view showing a source/drain region in FIG. 3;

FIGS. 5 and 6 are cross-sectional views illustrating a method for forming a semiconductor device according to the present invention;

FIG. 7 is a schematic cross-sectional view illustrating an apparatus for pre-cleaning a substrate according to the present invention;

FIG. 8 is a flow chart illustrating a method for pre-cleaning the substrate according to the present invention;

FIG. 9 is an enlarged cross-sectional view illustrating a RF etching method performed with respect to a contact hole in FIG. 6;

FIGS. 10 and 11 are cross-sectional views illustrating the method for manufacturing the semiconductor device according to the present invention;

FIG. 12A is a graph illustrating the increase of particles (P/C adders) relative to the number of wafers according to the present invention; and

FIGS. 12B and 12C are graphs illustrating the augments of particles relative to the number of wafers according to the conventional method

<Explanations of Reference Numerals in Principal Portions of Drawings>

10 : substrate	20 : source/drain region
22 : metal silicide layer	30 : insulation interlayer
34 : oxide layer	120 : electrode region
122 : metal silicide layer	130 : insulation interlayer
132 : contact hole	134 : oxide layer
200 : pre-cleaning unit	205 : housing
210 : processing chamber	220 : ICP unit
230 : bias unit	240 : pump
250, 252 : MFC	270 : quartz belljar
275 : quartz mask	

[DETAILED DESCRIPTION OF THE INVENTION]

[PROPOSE OF THE INVENTION]

[THE AREA TO WHICH THE INVENTION PERTAINS AND THE PRIOR ART]

The present invention relates to a method for cleaning a processing chamber used for manufacturing a semiconductor device and a method for manufacturing the semiconductor device by employing the same, and more particularly, relates to a method for cleaning a processing chamber by removing impurities on a semiconductor substrate and in the processing chamber before a chemical vapor deposition process, and a method for manufacturing a semiconductor device by employing the same.

As semiconductor devices are highly integrated, design rules, for example the channel lengths of transistors, the intervals of active regions, the widths of wirings, the intervals of wirings, and the sizes of contact holes, have been reduced. Therefore, the aspect ratio of a contact hole formed on a semiconductor substrate gradually increases.

The aspect ratio of the contact hole indicates the ratio of a depth of the contact hole relative to the diameter of the contact hole.

Accordingly, the conventional wirings and the interconnection films including aluminum (Al) deposited by a sputtering process, have several disadvantages as follows.

For example, the contact resistance of the wiring or the connecting film may be increased in accordance with the high integration degree of the semiconductor device while the step coverage of the deposited film may be deteriorated. Thus, the wirings and the connecting films may be frequently broken at the windows of the contact holes. Also, the connecting film including aluminum (Al) may be broken due to electro-migration during the performance of the semiconductor device.

Considering the above-mentioned problems, there are provided various metal plugs including metals for electrically connecting a conductive layer to an underlying conductive layer. In this case, a contact hole is formed through an interlayer dielectric film interposed between an upper and a lower conductive layers, and then a metal plug fills the contact hole to electrically connect the upper conductive layer to the lower conductive layer.

Generally, a metal plug including tungsten (W) has good step coverage, and is formed using a plasma enhanced chemical vapor deposition (PECVD) process.

FIG. 1 is a cross-sectional view illustrating a semiconductor device including contact holes. In FIG. 1, metal plugs are formed in contact holes by a deposition process after the contact holes are formed through an interlayer dielectric film 30.

Referring to FIG. 1, an active region and a field region 15 are defined ion a semiconductor substrate 10, and then the interlayer dielectric film 30 is formed on the substrate 10.

Source/drain region 20 having predetermined patterns is formed in the substrate 10

beneath the interlayer dielectric film 30. The source/drain region 20 is formed through an ion implantation process in which metals are implanted into the substrate 10.

A metal silicide film 22 is formed on the semiconductor substrate 10 to improve the electric conductivity between the source/drain region 20 and a metal plug 50. A contact hole is formed through the interlayer dielectric film 30 by an etching process to expose the metal silicide film 22.

Then, titanium (Ti) and titanium nitride (TiN) films 40 and 45 are deposited on the interlayer dielectric film 30 including the contact hole. The titanium film and the titanium nitride films 40 and 45 serve together a barrier layer. Tungsten is deposited in the contact hole where the titanium and titanium nitride films 40 and 45 are formed in order to form the metal plug 50. At that time, the titanium film 40 is formed in the contact hole and on the interlayer dielectric film 30 by a chemical vapor deposition (CVD) process or a sputtering process. In addition, the titanium nitride film 45 is formed on the titanium film 40 by a CVD process or a sputtering process.

Meanwhile, the metal silicide layer 22 is formed on the source/drain region 20 to reduce the contact resistance between the metal plug 50 and the source/drain region 20. That is, the metal silicide layer 22 serves as an ohmic layer so as to reduce the contact resistance between the source/drain region 20 and the metal plug 50. Also, the metal silicide layer 22 works as a diffusion barrier layer that can prevents materials from mutually diffusing between a metal layer and a semiconductor substrate or between two metal layers of a multi-layered construction.

The metal silicide layer 22 generally includes metal silicide such as titanium silicide ($TiSi_2$), platinum silicide ($PtSi_2$), lead silicide ($PdSi_2$), cobalt silicide ($CoSi_2$), or nickel silicide ($NiSi_2$). Because the cobalt silicide is stable at the high temperature of about 900°C. a

doped glassy film for planarization can be sufficiently formed on the cobalt silicide. Additionally, because the cobalt silicide has a low resistance of approximately 16 to 18 μΩ·cm, the silicide cannot be extended on the semiconductor substrate along the horizontal and the vertical directions. As a result, the source/drain may not be short concerning a gate electrode. Furthermore, the cobalt silicide can be selectively etched, and is not excessively etched during a plasma etching process in comparison with the titanium silicide.

However, a native oxide film may be easily formed on the cobalt silicide comparing to the titanium silicide such that the oxide film prevents the formation of the cobalt silicide or the cobalt silicide may have poor electrical contact relative to the metal formed thereon due to the oxide film. Thus, the surface of the cobalt silicide layer should be cleaned by a cleaning process.

FIGS. 2 and 3 are sectional views illustrating the conventional method for forming a tungsten plug.

Referring to FIG. 2, after a passivation layer 24 including a photo resist or an oxide is formed on a semiconductor substrate 10, the passivation layer 24 is partially etched in accordance with a predetermined pattern, thereby exposing predetermined region of the substrate 10, for example, a source/drain region.

Impurities including metal are implanted into the exposed region of the substrate 10 such that the source/drain region are formed on the substrate 10. Successively, the metal for forming a metal silicide film 22 is deposited on the source/drain region by a chemical vapor deposition (CVD) process or an ion implantation process. Then, the metal reacts with silicon at high temperature so that the metal silicide film 22 is formed on the source/drain region. Preferably, titanium (Ti) or cobalt (Co) can be employed to form the metal silicide film 22. The titanium or cobalt can react with the silicon of the substrate 10 to form a

titanium silicide ($TiSi_2$) film or a cobalt silicide ($CoSi_2$) film.

Referring to FIG. 3, after the remaining passivation layer 24 is removed, an interlayer dielectric film 30 is formed on the semiconductor substrate 10 including the metal silicide film 22 formed thereon.

A photo resist pattern for forming a contact hole 32 is formed on the interlayer dielectric film 30 by a photolithography process, and then the source/drain region is exposed through an etching process, thereby forming the contact hole 32. In this case, an oxide film 34 may be formed on the metal silicide film 22 exposed through the contact hole 32 after the etching process for forming the contact hole 32 is performed. In addition, impurities including etched by-products may exist on the metal silicide film 22. Because the semiconductor substrate 10 generally goes through several manufacturing processes to complete a semiconductor device, the semiconductor substrate 10 may contact with an air when the semiconductor substrate 10 is transferred from one processing chamber to another processing chamber. At that time, the oxide film 34 may be formed on the substrate 10 by contacting the substrate 10 with the air. Though a minute oxide film 34 is interposed between the source/drain region 20 and the metal plug 50, the electrical contact between the source/drain region 20 and the metal plug 50 becomes poor.

Accordingly, the oxide film 34 and the remaining impurities in the contact hole 32 should be removed from the substrate 10 before depositing other films for the plug 50 in the contact hole 32. The process for removing the oxide film 34 and remaining impurities is called as a pre-cleaning process.

The pre-cleaning process has been provided to remove oxide films and other impurities from the substrate before the CVD process for depositing titanium and titanium nitride. For example, in Unity-EP (manufactured by Tokyo Elctoron Co. in Japan) for

depositing a titanium/titanium nitride film employing a CVD process, the titanium/titanium nitride film is deposited after the pre-cleaning process is executed. When the metal silicide film includes cobalt silicide, the substrate is generally pre-cleaned with a discrete apparatus by employing a radio frequency (RF) plasma etching process ex-situ, and then the pre-cleaned substrate is introduced in a processing chamber for performing a CVD process.

In the meantime, the Unity-EP can have an additional function by installing a adequate processing module. Also, the Unity-EP can perform the pre-cleaning process in-situ by installing a Pre-Cleaning Etching Module (PCEM) therein. When the pre-cleaning is executed in-situ, the processing time can be reduced, and the throughput can be improved.

In the conventional pre-cleaning method, a plasma etching process is performed in a processing chamber with an argon (Ar) gas. However, when the pre-cleaning method is performed with the argon gas through a dry etching process, several disadvantages may occur as fallows.

FIG. 4 is an enlarged cross-sectional view showing the surface of the source/drain region in FIG. 3 in order to describe the disadvantages of the conventional methods.

As shown in FIG. 4, the metal silicide film 22 is damaged when the RF plasma etching process is excessively performed with the argon gas. In other words, the conventional methods may cause the problem that the metal silicide layer 22 is also removed with an oxide film and other impurities during the RF plasma etching process.

It is very difficult to precisely control the RF etching process without etching the metal silicide film 22. Also, the time may be disadvantageously increased when the etching process is executed by controlling the etched amount of the metal silicide film 22.

Furthermore, the manufacturing cost of a semiconductor device may be increased while the yield of the semiconductor device may be reduced. In fact, the cobalt silicide film is removed with the oxide film and the impurities by identical rate when the oxide film and the impurities are removed from the substrate during the etching process. As a result, processing failures may be caused due to the loss of the cobalt silicide film.

[TECHNICAL OBJECT OF THE INVENTION]

The present invention has been made to solve the afore-mentioned problems and accordingly, it is a first object of the present invention to provide a method for cleaning a processing chamber, which can minimize the damage of a metal silicide film by improving the etching selectivity of an oxide film relative to the metal silicide film.

It is a second object of the present invention to provide a method for cleaning a processing chamber, which can prevent particles fro generating in the processing chamber.

It is a third object of the present invention to provide a method for manufacturing a semiconductor device by employing an improved process for cleaning a processing chamber.

[CONTRUCTION AND OPERATION OF THE INVENTION]

To achieve the first object of the present invention, according to a method for cleaning a processing chamber of a preferred embodiment, after impurities are removed from a semiconductor substrate in the processing chamber with a plasma of a first gas including a hydrogen gas, the semiconductor substrate is removed from the processing chamber. Then, the processing chamber is etched with a plasma of a non-hydrogenous second gas. In this case, non-hydrogenous second gas does not include a hydrogen gas.

To achieve the second object of the present invention, according to a method for cleaning a processing chamber of anther preferred embodiment, a semiconductor

substrate is positioned on a stage in the processing chamber, an then the processing chamber is vacuumized. After a first gas is flowed into the processing chamber wherein the first gas includes an argon gas and a hydrogen gas, impurities are removed on the semiconductor substrate with a plasma of the first gas. Then, a gas is exhausted from the processing chamber, and the semiconductor substrate is removed from the processing chamber. Subsequently, the processing chamber is vacuumized, and a non-hydrogenous second gas is flowed into the processing chamber. Then, the processing chamber is etched with a plasma of the second gas.

To achieve the third objects of the present invention, according to a method for manufacturing a semiconductor device of another preferred embodiment, after a semiconductor substrate is positioned in a processing chamber, impurities are removed from the semiconductor substrate in the processing chamber with a plasma of a first gas including a hydrogen gas. The semiconductor substrate is removed from the processing chamber, and then the processing chamber is etched with a plasma of a non-hydrogenous second gas.

Preferably, the first gas includes an argon gas and a hydrogen gas. An oxide is selectively etched relative to a metal silicide film by performing the plasma etching with the first gas including the hydrogen gas.

However, during performing the plasma etching with the hydrogen gas, some hydrogen molecules and other materials react one after another to form atomic groups, e.g. radicals and the like. The radicals may easily react with a neighbor reactant such that new chemical compound can be formed. Those radicals or chemical compound having hydrogen may influence on the surroundings when other semiconductor substrates are treated, and also the radicals and the compound may cause particles on the substrate.

In other words, the excited radicals having hydrogen may react not only with cobalt (Co), silicon (Si) and silicon oxide (SiO_2) of the substrate but also with a quartz belljar disposed over the substrate and a quartz mask where the substrate is positioned. More particularly, the excited radicals may react with silicon oxide included in the quartz belljar or the quartz mask, and may remain in the processing chamber as the phase of the chemical compound. The remaining chemical compound in the processing chamber may fall on or adhere to other substrates, thereby generating the particles on the substrates when other substrates are treated in the processing chamber.

According to the present invention, after a fist RF plasma etching process is performed with the first gas, the semiconductor substrate is removed form the processing chamber. Then, a second RF plasma etching process is executed with the second gas in order to remove hydrogen from the processing chamber. At that time, the second gas does not include hydrogen, and the second gas preferably includes the argon gas.

Hereinafter, the reaction mechanism of hydrogen (H_2) in a processing chamber will be primary described.

Reaction Mechanism of Hydrogen

In general, before titanium (Ti) and titanium nitride (TiN) are deposited on a substrate, a pre-cleaning process is performed in-situ in an apparatus for a CVD process (for example, the Unity-EP) in which a PCEM is installed. When the pre-cleaning process is executed in-situ, the throughput of the process can be improved. Also, an undesired oxide film can be advantageously etched from the substrate by excellent etching selectivity using an argon (Ar) gas and a hydrogen gas. A radio frequency plasma etching process is performed in the PCEM by employing an induced coupled plasma (ICP) corresponding to

high density plasma.

After a mixture of the argon gas and the hydrogen gas is introduced in the processing chamber, electric power is applied from an ICP device to excite the mixture. Then, bias power is applied to a stage on which a wafer is positioned, thereby starting the RF plasma etching.

The hydrogen gas introduced with the argon gas reacts with the oxide film on the substrate at the temperature of about 500°C so that the oxide film is removed from the substrate as H_2O phase. Meanwhile, the hydrogen gas reacts with cobalt included in a metal silicide layer on the substrate such that cobalt hydride (CoH_x) is deposited on the substrate.

The reactions among the oxide film, the hydrogen gas, and the cobalt silicide in the processing chamber are proceed as following equations:

$Si + 4H^+ \rightarrow SiH_4\uparrow$ ..... equation 1

$SiO_2 + 8H_2 \rightarrow SiH_4\uparrow + 2H_2O\uparrow$ ..... equation 2

$Co + xH \rightarrow CoH_x\downarrow$ ..... equation 3

According to the above-mentioned equations, the oxide film is reacted with the hydrogen to form a hydrogenous compound like SiH_4 or water (H_2O), thereby removing the oxide film from the substrate as the phase of SiH_4 or H_2O. On the other hand, the metal silicide including the cobalt silicide is deposited on the substrate such that the metal silicide is not removed during the etching process. That is, the oxide film is selectively etched relative to the cobalt silicide. Practically, when the hydrogen gas is employed in the plasma etching process, the etching selectivity between the oxide film and the cobalt silicide film is nearly ten times augmented

Hereinafter, the preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings. In the following drawings, like reference numerals identify similar or identical elements.

FIG. 5 and FIG. 6 are cross-sectional views illustrating a method for manufacturing a semiconductor device according to the present invention. FIGS. 5 and 6 show the formation of an oxide film removed through an etching process.

Referring to FIGS. 5 and 6, after a passivation layer 124 is formed on a semiconductor substrate 100 including an active region and a field region 105, the passivation layer 124 is patterned to expose the portion of the semiconductor substrate 100. Then, a source and drain region 120 is formed at the exposed portion of the substrate 100 by an ion implantation process.

Subsequently, a metal silicide film 122 is formed on the source and drain region 120 through a CVD process or an ion implantation process. Because the process for forming the metal silicide film 122 is substantially performed at high temperature, metal reacts with the silicon in the substrate 100 to form the metal silicide film 122 on the source and drain region 120. Preferably, a cobalt silicide ($CoSi_2$) film is formed on the source and drain region 120 using cobalt in order to minimize contact resistance. Other metals can be used to form the metal silicide film 122 on the source and drain region 120.

After the passivation layer 124 is removed, an interlayer dielectric film 130 is formed on the substrate 100 including the metal silicide film 122. Then, the interlayer dielectric film 130 is partially etched through a photolithography process in order to form a contact hole 132 exposing the source and drain region 120.

The substrate 100 is contacted with air when the substrate 100 is carried from one processing chamber to another processing chamber. At that time, an oxide film 134 is

formed on the source and drain region 120 and on the inside of the contact hole 132 as shown in FIG. 6. In addition, impurities like etched by-products remain on the source and drain region 102 and the inside of the contact hole 132 after the photolithography process is performed for forming the contact hole 132.

Before a titanium (Ti) film and a titanium nitride (TiN) film are deposited on the inside of the contact hole 132, the oxide film 134 and the impurities should be removed from the surfaces of the source and drain region 120 and the contact holes 132. A pre-cleaning process is executed to remove the oxide film 134 and the impurities from the substrate 100 before successive processes.

FIG. 7 is a schematic cross-sectional view illustrating an apparatus for pre-cleaning a substrate according to the present invention, FIG. 8 is a flow chart illustrating the method for pre-cleaning the substrate according to the present invention, and FIG. 9 is an enlarged cross-sectional view illustrating a RF etching method performed with respect to a contact hole in FIG. 6.

Referring to FIG. 7, a pre-cleaning apparatus 200 of the present invention includes a housing 205 enclosing a processing chamber 210, an ICP device 220 disposed over a semiconductor substrate 100 for providing a plasma, a RF bias device 230 disposed under the substrate 100, a pump 240 for forming a vacuum in the processing chamber 210, a quartz mask 275 where the substrate 100 is positioned, and a quartz belljar 270 disposed over the quartz mask 275 for providing a processing space in the processing chamber 210.

The quartz mask 275 and the quartz belljar 270 provide together the processing space in the processing chamber 210, and the substrate 100 is positioned on a stage provided by the quartz mask 275.

Also, supply tubes are connected to the pre-cleaning apparatus 200 in order to supply an argon gas and a hydrogen gas into the processing chamber 210, respectively. The supply tubes are connected to an argon supply source 254 and a hydrogen supply source 256, and a first mass flow controller (MFC) 250 and a second MFC 252 are installed in the supply tubes, respectively.

A first valve 261 is installed between the first MFC 250 and the argon source 254, and a second valve 262 is installed between the first MFC 250 and the pre-cleaning apparatus 200. In addition, a third valve 263 is installed between the second MFC 252 and the hydrogen source 256, and a forth valve 264 is installed between the second MFC 252 and the pre-cleaning apparatus 200.

Referring to FIGS. 7 to 9, after the substrate 100 having the contact hole is positioned on the quartz mask 275 (S10), pump 240 is operated to vacuumize the processing chamber 210 (S20). That is, the substrate 100 including an oxide film or remaining impurities is transferred into the processing chamber 210, and the substrate 100 is disposed in a processing space provided by the quartz mask 275 and the quartz belljar 270. Then, the pump 240 exhausts a gas in the processing chamber 210.

When the processing chamber 210 is maintained to have high vacuum, an argon gas and a hydrogen gas are introduced into the processing chamber 210 through the first and the second MFC 250 and 252 while the flow rates of the argon and hydrogen gases are controlled by the first and second MFC 250 and 252, respectively. The argon and hydrogen gas are mixed each other to form a first mixing gas, and then the first mixing gas is introduced into the processing chamber 210 (S30).

In the present invention, the flow rate of the argon gas relative to the hydrogen gas is approximately 1:0.8 to 1:1.2. According to one preferred embodiment of the present

invention, the first mixture gas includes the argon gas by approximately 5sccm (standard cubic centimeters per minute) and the hydrogen gas by approximately 5sccm. Namely, the flow rate ratio between the argon gas and the hydrogen gas is about 1:1. However, the ratio and the flow rate of the argon gas and the hydrogen gas in the first mixture gas can be varied in accordance with the processing chamber 210, the semiconductor substrate 100, or the processing conditions.

The ICP device 220 and the bias device 230 activate the first mixture gas to form a plasma in the processing chamber 210, and then the plasma generated form the first mixture gas reacts with the oxide film or the impurities on the substrate 100 when a first RF etching process is executed (S40).

As shown in FIG. 9, chemical reactions of the oxide film, the impurities, the metal oxide film 122, and the hydrogen are performed during the first RF etching process while the oxide film and the impurities are etched by employing the argon in the plasma.

The processing space in the processing chamber 210 is maintained to have the temperature of approximately 450~550°C during the first RF etching process, thereby accelerating the above-mentioned chemical reactions.

As it is described above, the hydrogen reacts with silicon (Si) and silicon oxide (SiO_x) to form silane (SiH_4) and water (H_2O) so that the silicon and the silicon oxide can be removed from the substrate 100 as the phases of silane (SiH_4) and water (H_2O). Simultaneously, cobalt (Co) included in the metal silicide film 122 reacts with the hydrogen to form cobalt hydride (CoH_x) such that the cobalt hydride is deposited on the source and drain region 120 of the substrate 100. As a result, the cobalt can remain on the source and drain region 120 of the substrate 100. That is, according to the aforementioned equations 1, 2 and 3 such as $Si + 4H^+ \rightarrow SiH_4 (\uparrow)$, $SiO_2 + 8H_2 \rightarrow SiH_4 (\uparrow) + 2H_2O (\uparrow)$, and $Co + xH \rightarrow$

CoH_x ($\downarrow$), the first RF etching process is achieved to remove the oxide film and the impurities from the substrate 100 using the plasma generated form the first mixture gas including the argon and the hydrogen gases.

When first RF etching process is performed for predetermined time, the performances of the ICP and the bias devices 220 and 230 are stopped, thereby completing the first RF etching process.

After the first RF etching process, the first and the third valves 261 and 263 are closed, the pump 240 is operated to completely exhaust the first mixture gas from the processing chamber 210 and the first and the second MFC 250 and 252 (S50).

After the substrate 100 is removed from the processing chamber 210, the substrate 100 is transferred for successive processes (S60). Then, the pump 240 operates to vacuumize the processing chamber 210 (S70).

When the first MFC 250 operates and the first and the second valves 261 and 262 are open, a second gas including an argon gas is flowed into the processing chamber 210 (S80). At that time, because the third and the forth valves 263 and 264 are closed, a hydrogen gas cannot be introduced into the processing chamber 210.

After the second gas is introduced into the processing chamber 210, RF energy is applied to the second gas to generate a argon plasma, thereby starting a second RF etching process (S90).

During the first RF etching process, the hydrogen reacts with the silicon, the silicon oxide, and the cobalt. At the same time, a hydrogen radical collides with the quartz belljar 270 and the quartz mask 275. Thus, reaction by-products remains in the processing chamber 210 while another compound is generated during the reactions of the hydrogen and the quartz (silicon oxide) in the quartz belljar 270 and the quartz mask 275. The

compound may remain on the quartz belljar 270 and on the quartz mask 275 when the first mixture gas is exhausted from the processing chamber 210 after the first RF etching process.

When the remaining compound of the hydrogen and the quartz may be gradually accumulated in the processing chamber 210, the accumulated compound becomes the particles formed on the substrate after predetermined numbers of substrates are treated in the processing chamber 210. The particles can cause the failure of the semiconductor device formed on the substrate, and the throughput of the semiconductor substrate decreases due to the particles.

To overcome the aforementioned problem, according to the pre-cleaning method of the present invention, a second gas without the hydrogen gas (namely, non-hydrogenous) is flowed into the processing chamber 210 after the substrate 100 is removed from the processing chamber 210. Then, the second RF etching process is performed with the plasma generated from the second gas. After the second RF etching process is completed, the pump 240 is operated to exhaust the gas from the processing chamber 210.

FIGS. 10 and 11 are cross-sectional views illustrating the method for manufacturing the semiconductor device according to the present invention.

The metal silicide film 122 of the substrate 100 is not damaged during the RF etching processes for removing the oxide film 134 and the impurities.

Referring to FIG. 10, after titanium and titanium nitride (TiN) are successively deposited on the source and drain region 120 and on the inside the contact hole 132 such that a titanium and a titanium nitride films are formed. The titanium and the titanium nitride films serve together as a metal barrier layer. Then, tungsten is deposited on the titanium

and the titanium nitride film by a plasma enhanced CVD (PECVD) process, thereby forming a tungsten plug 50.

Referring to FIG. 11, after the titanium and the titanium nitride films, and the tungsten plug 50 are successively formed, they are polished through a chemical and mechanical polishing (CMP) process or an etch back process so that the plug 50 is completed. In the present invention, the successive processes for forming the semiconductor device like a capacitor or a transistor are the same as those of the conventional method for forming the semiconductor device.

FIG. 12A is a graph illustrating the increase of particles (P/C adders) relative to the number of wafers according to the present invention, and FIGS. 12B and 12C are graphs illustrating the augments of particles relative to the number of wafers according to the conventional method. In FIGS. 12B and 12C, the augments of the particles are obtained in accordance with processing conditions varied in each step.

Referring to FIG. 12A, approximately ten particles are advantageously increased when the pre-cleaning process of the present invention is performed concerning the wafers. That is, the P/C adders are approximately 10 according to the present invention. In other words, the P/C adders according to the present are remarkably lower than that of the conventional method shown in FIGS. 12B 12C.

In FIG. 12A, the increase of the particles are obtained through the second RF etching process after the first RF etching process is performed using the plasma generated from the first gas mixture of the argon and the hydrogen gases. At that time, the flow rates of the argon and the hydrogen gas are approximately 5sccm in the first RF etching process. After the first RF etching process, the second RF etching process proceeds in case that the

electric power of the ICP device is about 500W and the electric power of the bias device is about 50W during the second RF etching process (the condition of AFTER-V4).

As shown in FIG. 12A, the P/C adders are considerably increased when the numbers of the wafers is about 620, about 1,000, and about 1,100. At those points, the particles are increased because the conventional process is executed concerning the related wafers in order to identify the effect of the present invention.

Referring to FIG. 12B, the augment of the particles can be obtained under the processing conditions as follows.

In the processing condition of C1-1, a first RF etching process is performed with a first mixture gas including an argon gas and an hydrogen gas, and then a remaining mixture gas in a processing chamber and a MFC is exhausted by pumping without a second RF etching process. During performing the first RF etching process with the first gas, the processing chamber is maintained at the high temperature of about 500°C so that the processing chamber is generally preheated (referred as a heat-up step) before the etching process.

In the processing condition of C1-2, the step of preheating the processing chamber is omitted to restrain particles generated from the hydrogen gas, and the mixture gas is exhausted from the processing chamber and the MFC by pumping without a second RF etching process.

As for the processing condition of C1-3, the flow rate of the hydrogen gas was 0sccm during the first RF etching process. That is, the hydrogen gas does not used in the first RF etching process. However, because the radicals including hydrogen exist in a quartz belljar and a quartz mask, particles are generated on the wafer though the first RF etching process is executed without the hydrogen gas.

According to the processing condition of C1-4, the first RF etching process is performed when the temperature is reduced from approximately 500°C to approximately 200°.

In the processing condition of C1-5, the first RF etching process is executed using the first mixture gas including the argon and the hydrogen gases while the etching process is performed by employing the argon gas only in accordance with the conventional processing condition like argon-based etching process.

With the processing condition of C1-6, the first RF etching process is performed in accordance with the processing condition of C1-5 but the step of preheating the processing chamber is omitted according to the processing condition of C1-2.

As for the processing condition of C1-7, the first RF etching process is substantially performed in accordance with the processing condition of C1-5, however, the step of preheating the processing chamber is performed.

In the processing a condition of C1-8, the first RF etching process is performed using the plasma generated from the first mixture gas including the argon and the hydrogen gases. Then, the quartz mask including the wafer positioned thereon is etched with the plasma of the argon gas. During etching the quartz mask, the electric power of about 500W is applied to the ICP device, and also the electric power of about 400W is applied to the bias device (referred as AFTER-V3).

In the processing condition of C1-9, the first RF etching process and the quartz mask etching process are performed in accordance with the processing condition of C1-8 (AFTER-V3), however, the electric power is not applied to the bias device in order to minimize the damage of the quartz included in the quartz belljar and the quartz mask (referred as AFTER-V2).

As for the processing condition of C1-10, the first RF etching process is performed using the first mixture gas including the argon and the hydrogen gas in accordance with the conventional processing condition like the argon-based etching in which the etching process is executed the argon gas only. However the second RF etching process is performed according to the processing condition of C1-8.

Table 1

No.	mark in drawings	detail condition	Ref.
C1-1	Ar/H_2 STD	after Ar/H_2 plasma etching, pumping the chamber and the MFC	AFTER-V1
C1-2	heat-up skip	before Ar/H_2 plasma etching, skipping a heat-up step	
C1-3	w/o H2	the first RF etching without H_2	
C1-4	500 →200°C	the first RF etching performed at a temperature of about 200°C	
C1-5	Ar-base	employing the conventional processing condition using only H_2	
C1-6	Ar + heat-up skip	omitting the heat-up step under a condition of Ar Base	
C1-7	Ar + heat-up	applying the heat-up step under the Ar-based condition	
C1-8	quartz etch	after Ar/H_2 plasma etching, etching the quartz mask (ICP power of 500W and bias power of	AFTER-V3

		400W)	
C1-9	not etching quartz	bias power under the condition of AFTER-V3	AFTER-V2
C1-10	Ar+ quartz etch	employing the condition of Ar-based and AFTER-V3	

Referring to Table 1 and FIG. 12B, the P/C adders are remarkably greater than that shown in FIG. 12A though the processing conditions are varied. Hence, the second RF etching process of the present invention can be advantageously performed for preventing the particles from forming on the wafer.

Referring to FIG. 12C, the P/C adders are obtained in accordance with the following processing conditions.

In the processing condition of C2-1, the processes are performed in accordance with the condition of C1-1 (AFTER-V1).

According to the processing condition of C2-2, the electric power of approximately 50W is applied to the bias device, and the second RF etching process is performed for approximately 20 seconds.

As for the processing condition of C2-3, the electric power of approximately 60W is applied to the bias device in accordance with the condition of C2-2 in order to identify that the P/C adders depended on the electric power applied to the bias device.

In the processing condition of C2-4, the electric power of approximately 70W is applied to the bias device according to the condition of C2-2 in order to identify that the P/C adders depended on the electric power applied to the bias device.

With the processing condition of C2-5, the second RF etching process is performed for about 40 seconds in accordance with the condition of C2-2.

In the processing condition of C2-6, the second RF etching process is performed for about 60 seconds in accordance with the condition of C2-2.

In the processing condition of C2-7, the electric power of 0 W is applied to the bias device during the second RF etching process in accordance with the condition of C2-6. That is, the electric power is not applied to the bias device.

According to the processing condition of C2-8, the second RF etching process is performed for about 100 seconds in accordance with the condition of C2-6.

As for the processing condition of C2-9, the pumping process concerning the processing chamber and the MFC are performed for about 120 seconds in accordance with the condition of C2-2 (AFTER-V4).

In the processing condition of C2-10, the first RF etching process is performed at the temperature of approximately 200°C in accordance with the condition of C2-2 (AFTER-V4).

Table 2

No.	mark in drawings	detail condition	Ref.
C2-1	AFTER-V1	AFTER-V1	
C2-2	AFTER-V4 B50W, T=20	bias power is 50W under the condition identical to AFTER-V3 (AFTER-V4) and etching time is 20 seconds	
C2-3	V4, B60W, T=20	bias power is60W under the condition identical to AFTER-V4	
C2-4	V4, B70W, T=20	bias power is 70W	

		under the condition identical to AFTER-V4	
C2-5	V4, B50W, T=40	etching time is 40 seconds under the condition identical to AFTER-V4	
C2-6	V4, B60W, T=60	etching time is 60 seconds under a condition as same as AFTER-V4 (AFTER-V5)	
C2-7	V4, B0W, T=60	bias power is 0W under the condition identical to AFTER-V5	
C2-8	V4, B50W, T=100	etching time is 100 seconds under the condition identical to AFTER-V5	
C2-9	V4, B50W, T=60, vac=120	pumping time is100 seconds under the condition identical to AFTER-V4	
C2-10	V4, B50W, T=60 Temp=200°C	temperature is 200°C under the condition identical to AFTER-V4	

Referring to Table 2 and FIG. 12C, the P/C adders are remarkably higher than that shown in FIG. 12A though the processing conditions are varied. Thus, the second RF etching process of the present disclosure is very effective for restrain the particles on the substrate from generating.

[TECHNICAL EFFECT OF THE INVENTION]

According to the present invention, the first RF etching process using the first mixture gas including the hydrogen gas can improve the etching selectivity between the metal silicide and the oxide films. Thus, the damage of the source and drain region can be minimized, and the pre-cleaning process can be effectively performed.

Also, the second RF etching process of the present invention can be performed without the hydrogen gas so that the particles cannot be generated on the substrate.

Although exemplary preferred embodiments of the present disclosure have been described, it is to be understood that the present disclosure should not be limited to these preferred embodiments, but that various changes and modifications can be made by one skilled in the art while remaining within the spirit and scope of the present disclosure as hereinafter claimed.

What is claimed is:

1. A method for cleaning a processing chamber comprising:

removing impurities on a semiconductor substrate in the processing chamber with a plasma of a first gas including a hydrogen gas;

removing the semiconductor substrate from the processing chamber; and

etching the processing chamber with a plasma of a non-hydrogenous second gas.

2. The method of claim 1, wherein an inside of the processing chamber includes silicon oxide.

3. The method of claim 1, wherein the first gas includes the second gas and the hydrogen gas.

4. The method of claim 3, wherein the second gas includes an argon gas.

5. The method of claim 4, wherein a flow rate ratio between the argon gas and the hydrogen gas in the first gas is approximately 1:0.8 to1:1.2.

6. The method of claim 1, wherein the impurities on the semiconductor substrate are removed at a temperature of approximately 450 to 550°C.

7. A method for cleaning a processing chamber comprising:

positioning a semiconductor substrate on a stage in the processing chamber;

vacuumizing the processing chamber;

introducing a first gas into the processing chamber wherein the first gas includes an argon gas and a hydrogen gas;

removing impurities on the semiconductor substrate with a plasma of the first gas;

exhausting a gas from the processing chamber;

removing the semiconductor substrate from the processing chamber;

vacuumizing the processing chamber;

introducing a non-hydrogenous second gas into the processing chamber; and

etching the processing chamber with a plasma of the second gas.

8. The method of claim 7, further comprising a belljar is disposed over the stage, and a processing space provided by the belljar and the stage for positioning the semiconductor substrate, wherein at least one of the stage and the belljar includes silicon oxide.

9. The method of claim 7, wherein the impurities on the semiconductor substrate are removed at a temperature of approximately 450 to 550°C.

10. The method of claim 7, wherein the second gas includes an argon gas, and the first gas includes an argon gas and a hydrogen gas.

11. The method of claim 10, wherein a flow rate ratio between the argon gas and the hydrogen gas in the first gas is approximately 1:0.8 to 1:1.2.

12. A method for manufacturing a semiconductor device comprising:

positioning a semiconductor substrate in a processing chamber;

removing impurities on the semiconductor substrate in the processing chamber with a plasma of a first gas including a hydrogen gas;

removing the semiconductor substrate from the processing chamber; and

etching the processing chamber with a plasma of a non-hydrogenous second gas.

13. The method of claim 12, wherein the first gas includes the second gas and the hydrogen gas.

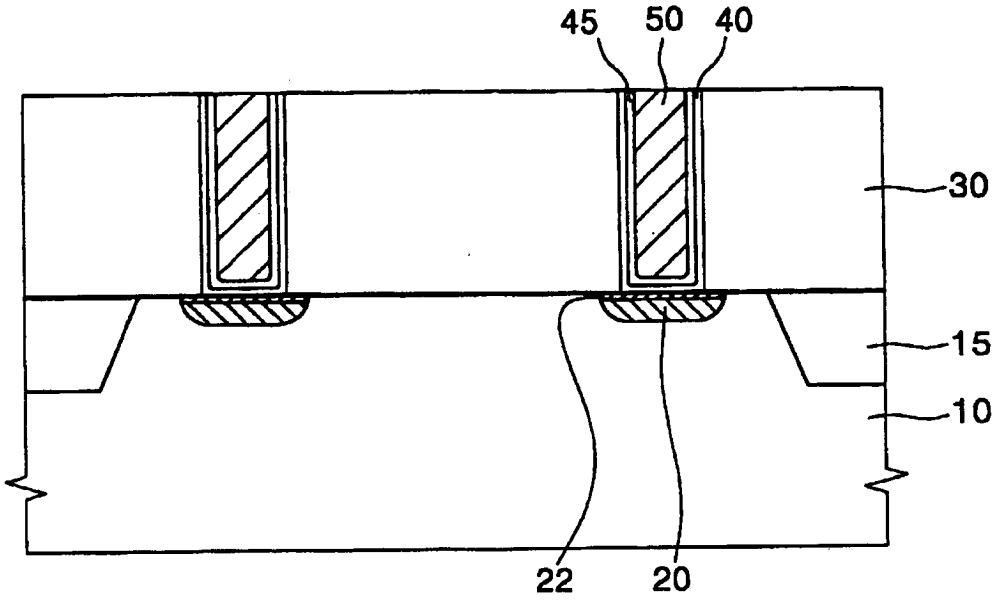
14. The method of claim 13, wherein the second gas includes an argon gas.

15. The method of claim 14, wherein a flow rate ratio between the argon gas and the hydrogen gas in the first gas is approximately 1:0.8 to 1:1.2.

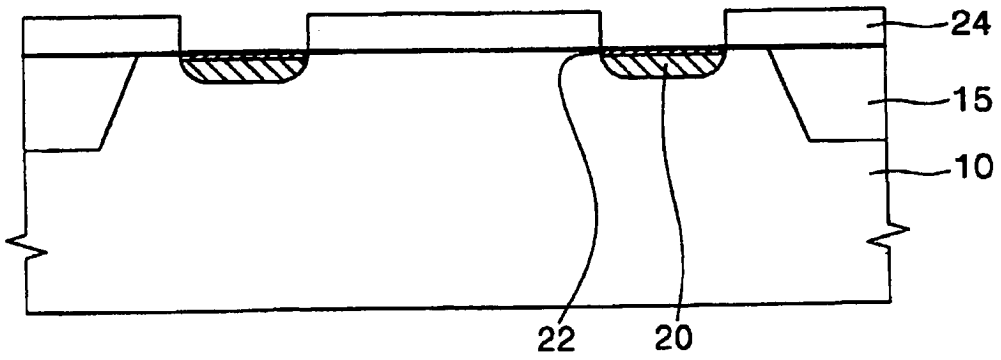
16. The method of claim 12, wherein the impurities on the semiconductor substrate are removed at a temperature of approximately 450 to 550°C.

[DRAWINGS]

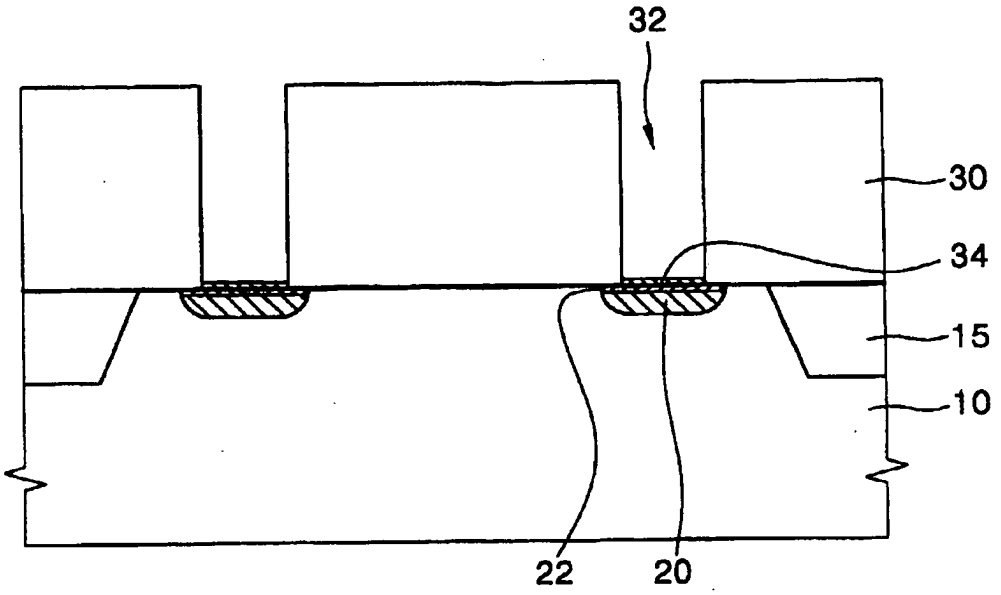
[FIG.1]



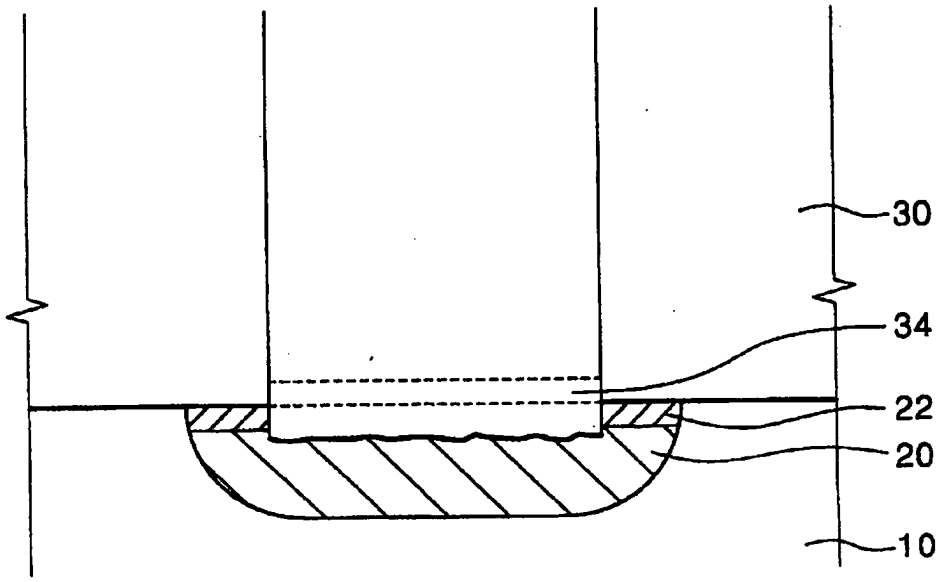
[FIG.2]



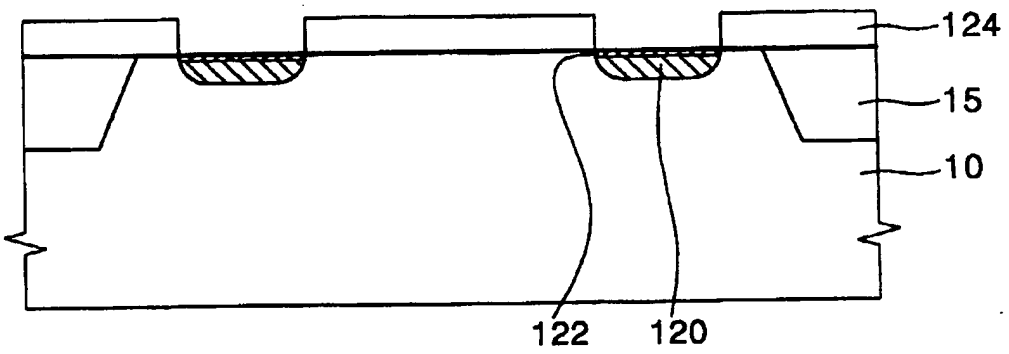
【FIG.3】



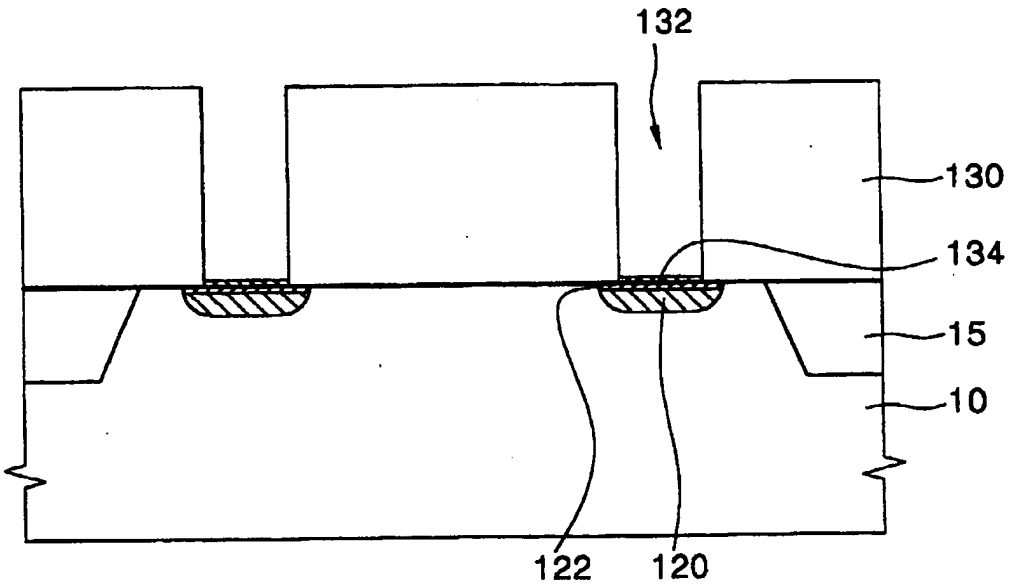
【FIG.4】



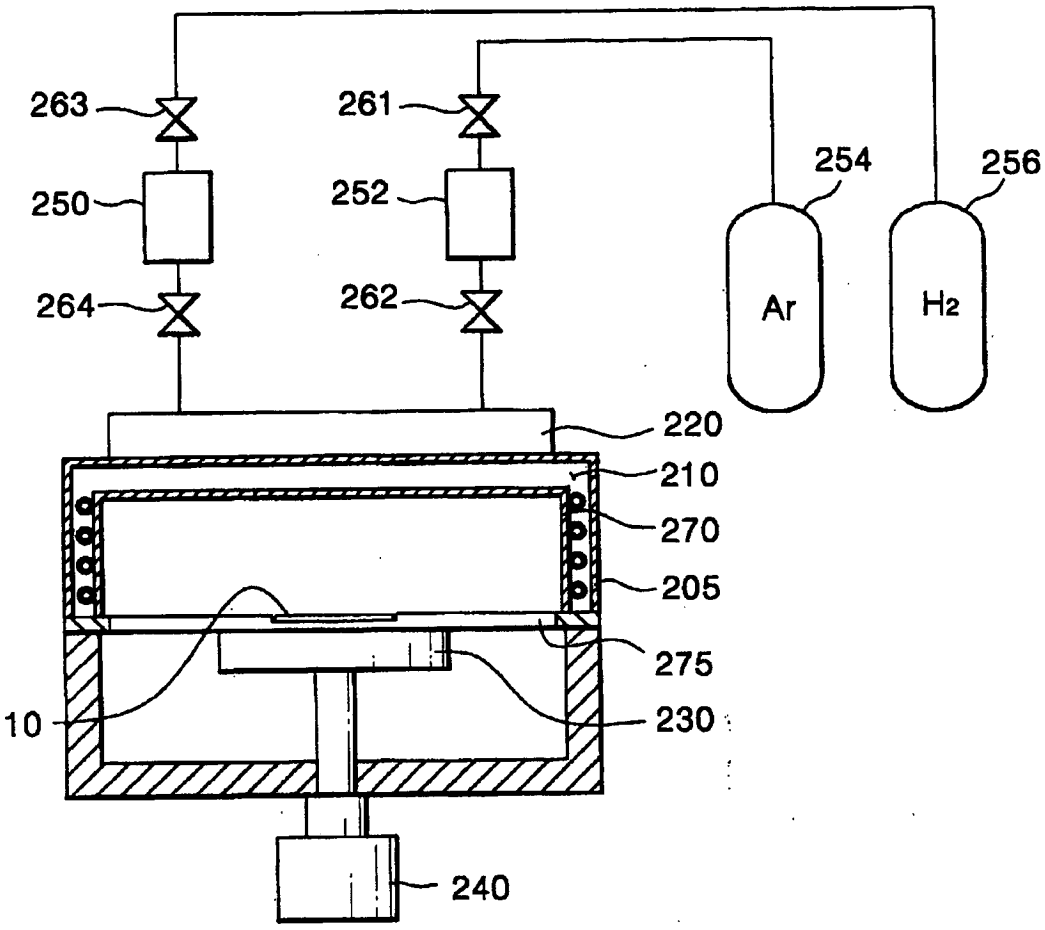
【FIG.5】



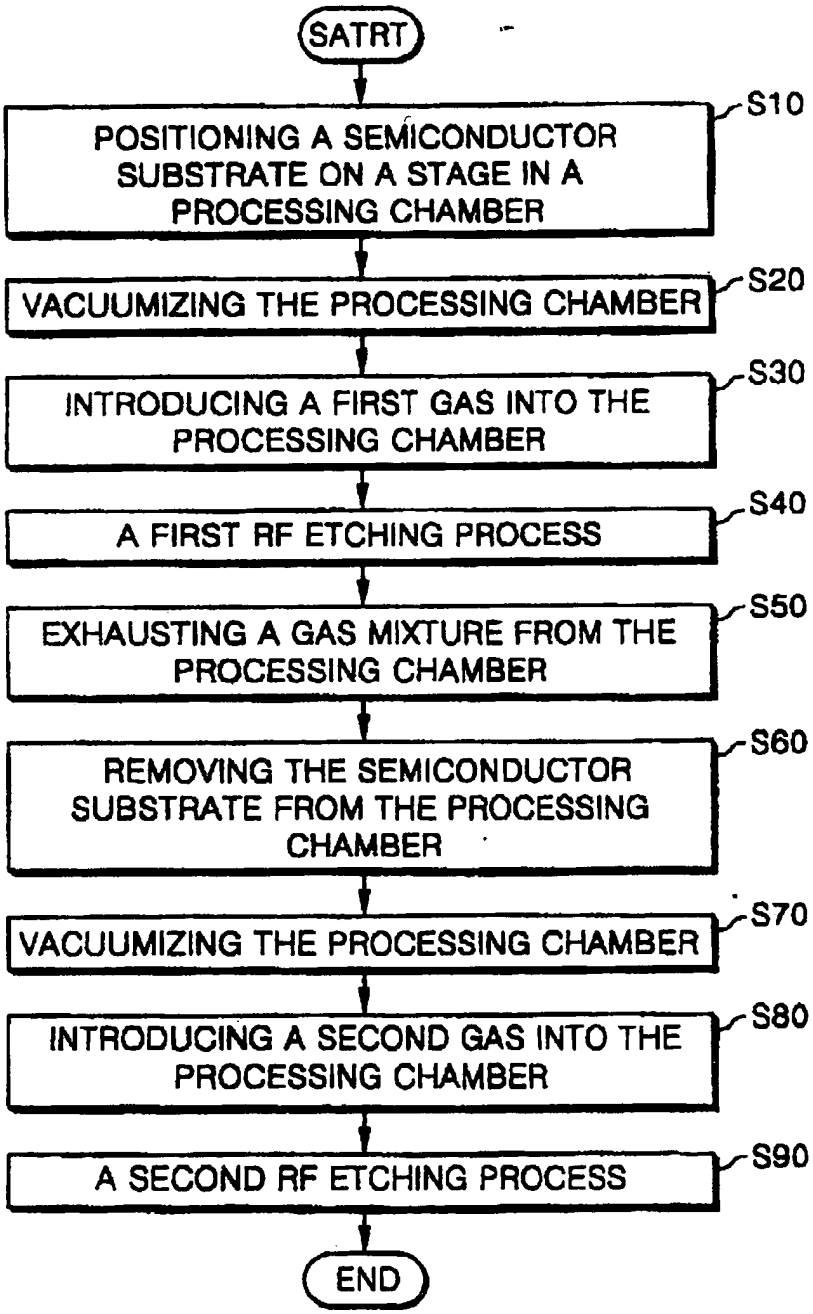
【FIG.6】



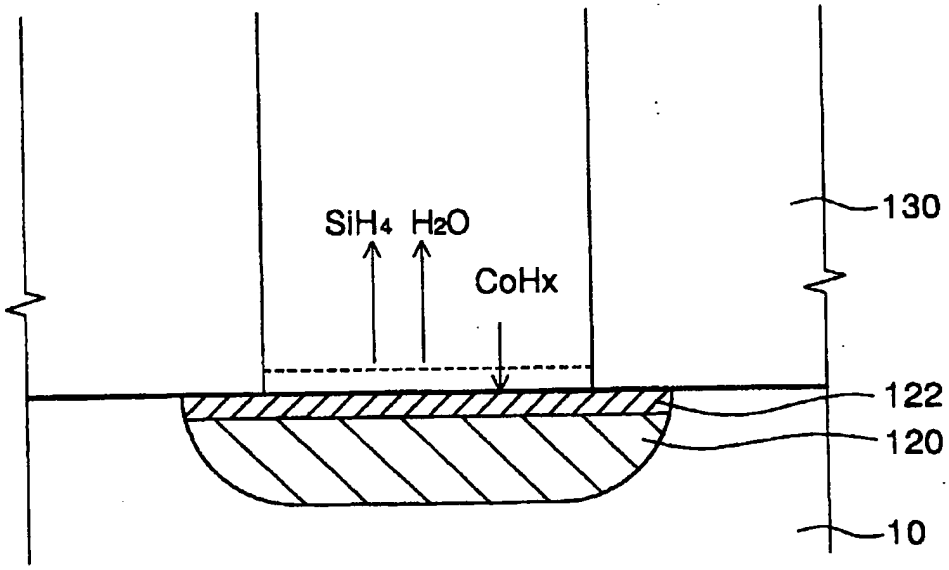
【FIG.7】


263
261
254
256
250
252
Ar
H2
264
262
220
210
270
205
275
10
230
240

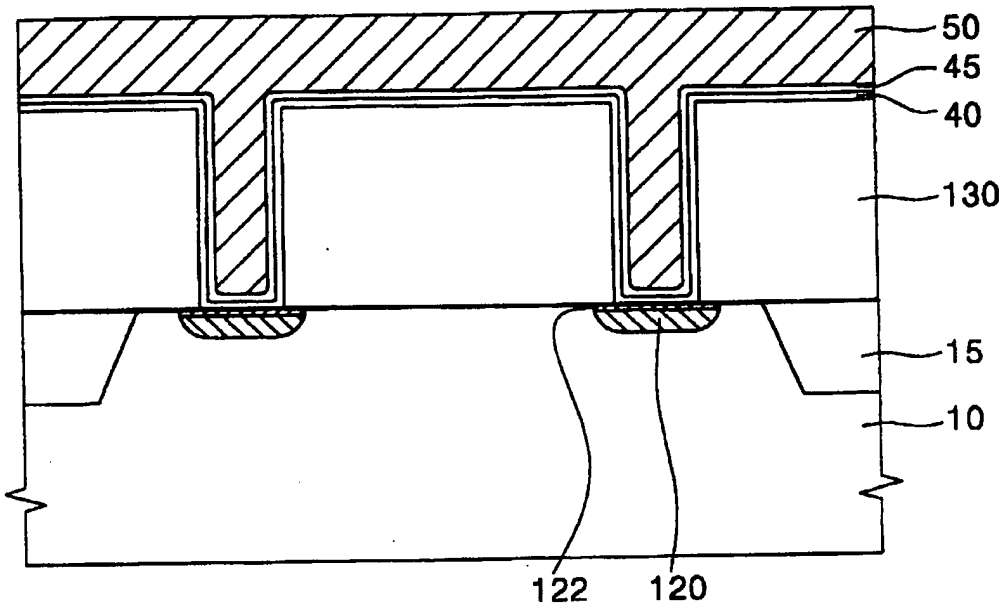
[FIG.8]


SATRT
POSITIONING A SEMICONDUCTOR SUBSTRATE ON A STAGE IN A PROCESSING CHAMBER
S10
VACUUMIZING THE PROCESSING CHAMBER
S20
INTRODUCING A FIRST GAS INTO THE PROCESSING CHAMBER
S30
A FIRST RF ETCHING PROCESS
S40
EXHAUSTING A GAS MIXTURE FROM THE PROCESSING CHAMBER
S50
REMOVING THE SEMICONDUCTOR SUBSTRATE FROM THE PROCESSING CHAMBER
S60
VACUUMIZING THE PROCESSING CHAMBER
S70
INTRODUCING A SECOND GAS INTO THE PROCESSING CHAMBER
S80
A SECOND RF ETCHING PROCESS
S90
END

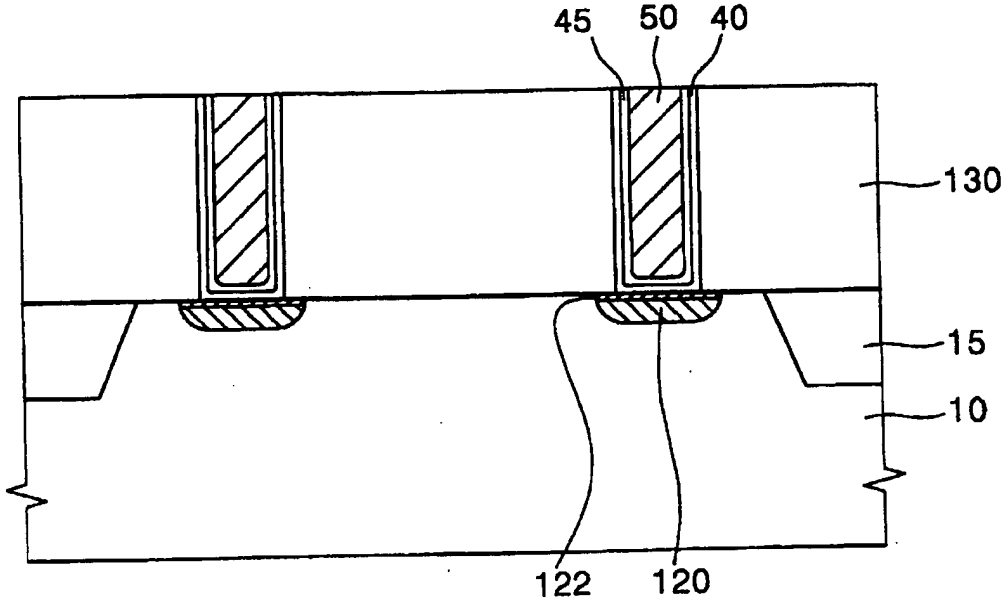
【FIG.9】



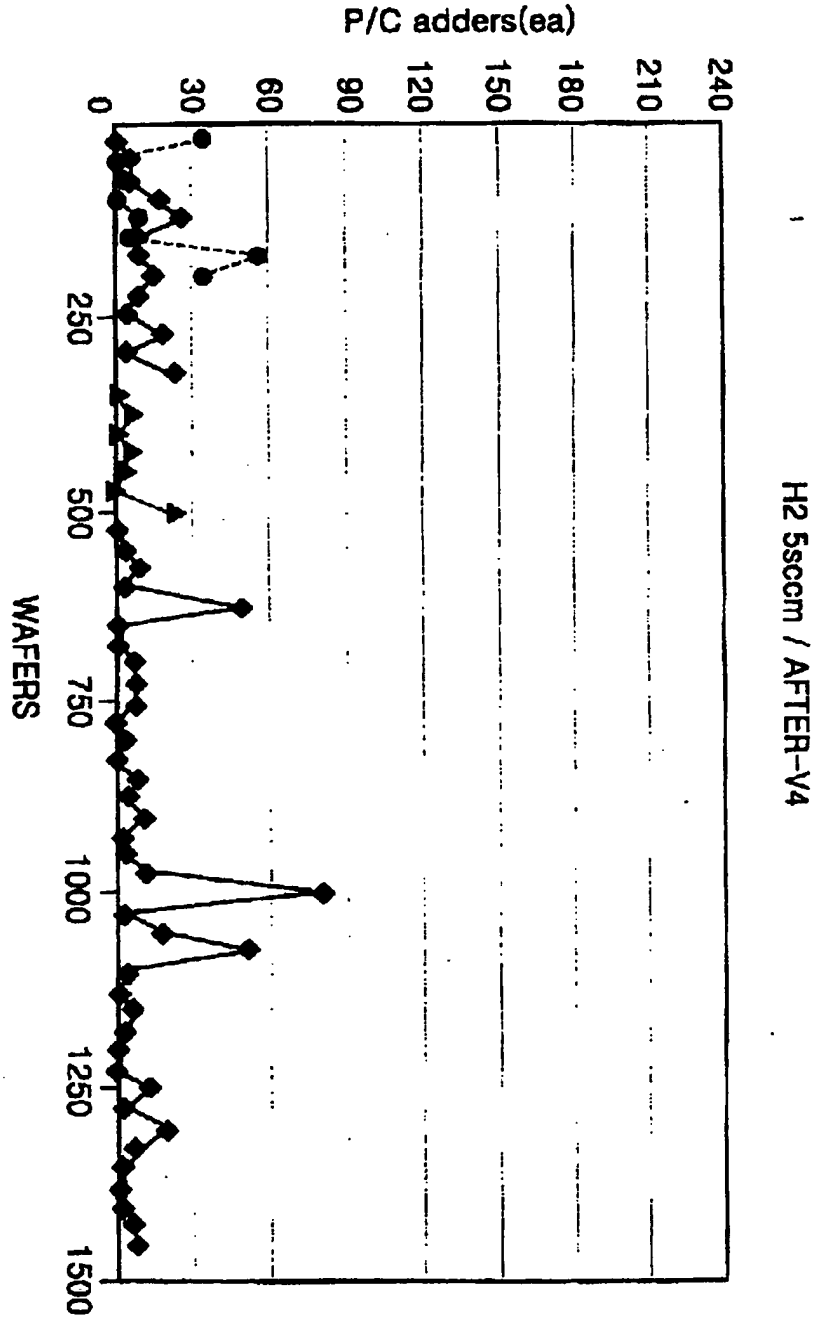
【FIG.10】



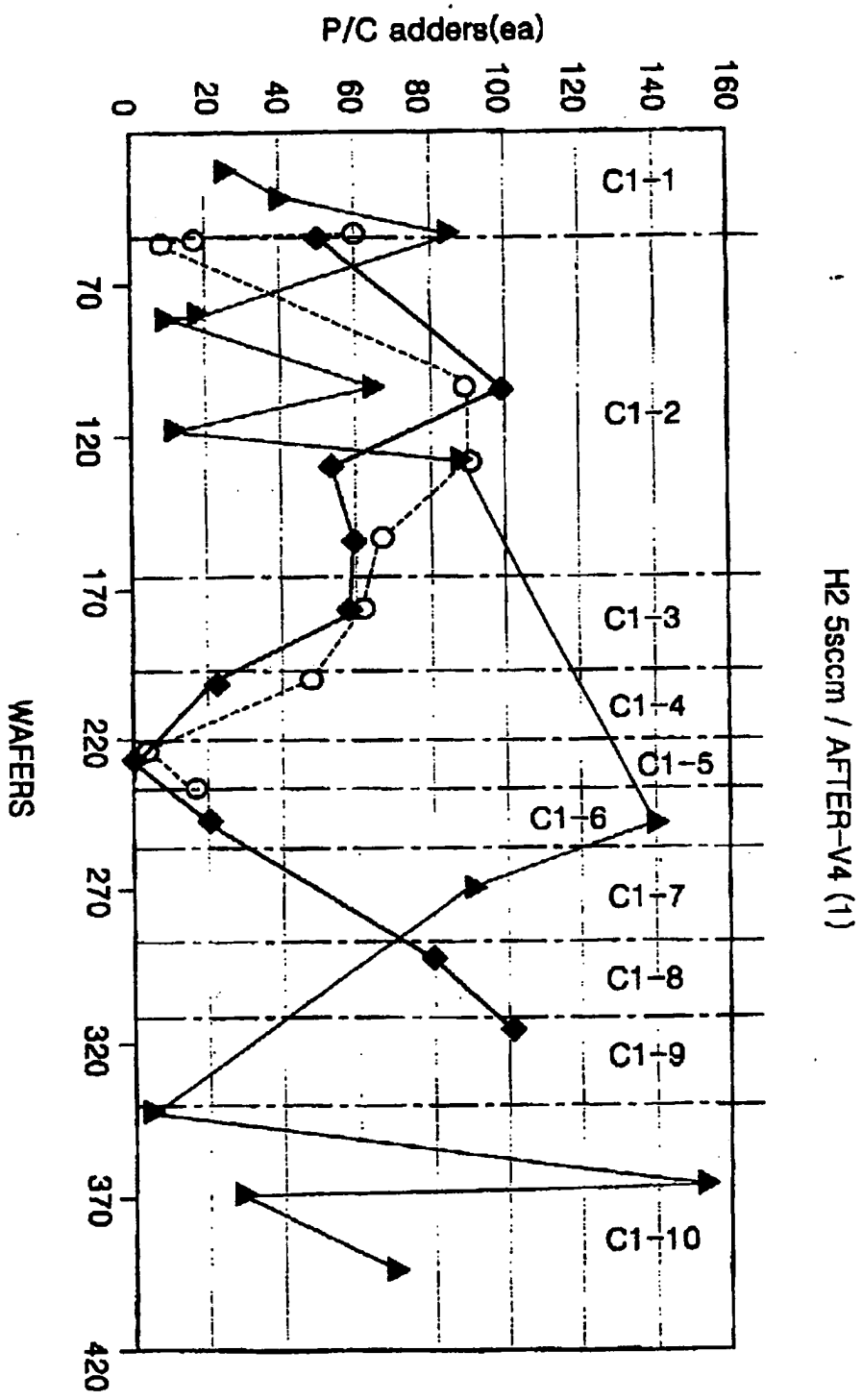
【FIG.11】



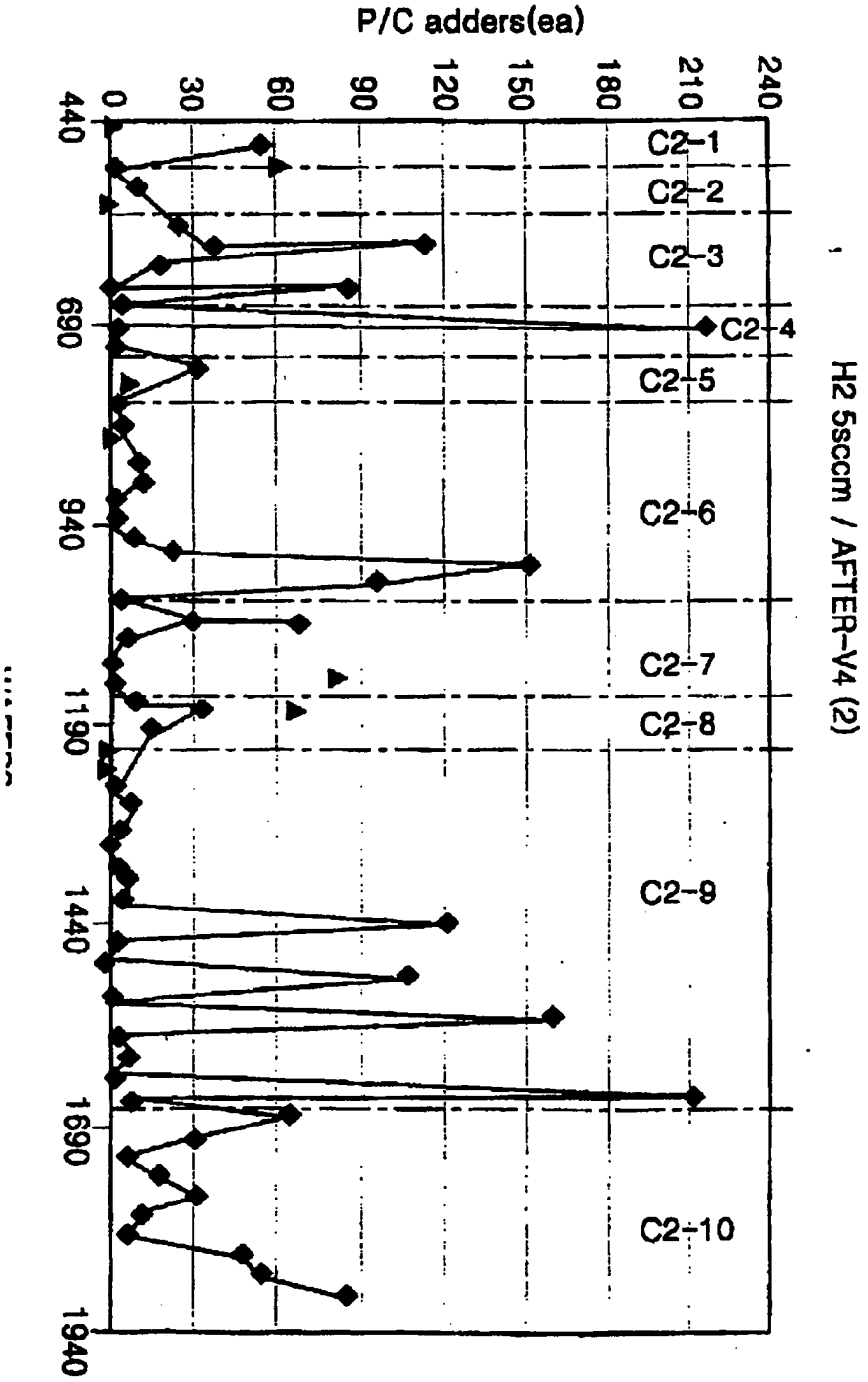
【FIG.12a】


P/C adders(ea)
0
30
60
90
120
150
180
210
240
WAFERS
0
250
500
750
1000
1250
1500
H2 5sccm / AFTER-V4

【FIG.12b】


P/C adders(ea)
0
20
40
60
80
100
120
140
160
WAFERS
70
120
170
220
270
320
370
420
C1-1
C1-2
C1-3
C1-4
C1-5
C1-6
C1-7
C1-8
C1-9
C1-10
H2 5sccm / AFTER-V4 (1)

[FIG.12c]


P/C adders(ea)
0
30
60
90
120
150
180
210
240
440
690
940
1190
1440
1690
1940
C2-1
C2-2
C2-3
C2-4
C2-5
C2-6
C2-7
C2-8
C2-9
C2-10
H2 5sccm / AFTER-V4 (2)

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